Culm 7-16-02

2826
#9
Amdt
a
8-1-02
ARJ

Serial No. 09/648,164

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks Washington, D.C. 20231 on 7-16-02

Mary V. Carter
Printed name of person mailing paper or fee

Mary V. Carter
Signature of person mailing paper or fee

Patent Application

Inventor(s): **Chyan, Yih Feng**
Hergenrother, John
Monroe, Donald

Case: **15-6-9**

Serial No.: **09/648164**

Filing Date: **August 25, 2000**

Examiner: **Dickey** **Group Art Unit: 2826**

Title: **Architecture for Circuit Connection Of A Vertical Transistor**

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D. C. 20231-

SIR:

Amendment Under 37 C.F.R.§1.111

In response to the office action of April 10, 2002, please amend the above-identified application as follows:

page 3, line 20
TAD 10/24/03

IN THE SPECIFICATION

(1) Please replace the sentence at ~~page 4, line 7~~ with the following: CMOS integrated circuits having PMOS transistors integrated with NMOS transistors are well known, and a process for fabricating CMOS vertical MOSFETs is described in U.S. Serial No. 09/335646 entitled, "A CMOS Integrated Circuit Having Vertical Transistors and a Process of Fabricating Same, " filed on June 18, 1999, now incorporated by reference.

a1 NE